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EXAMINER	
KIM, JAY C	
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2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,907	SUGIHARA ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment filed November 11, 2010.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-7, 11, 15-20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114) and further in view of Vijayakumar et al. (US 4,751,149) and still further in view of Wager et al. (US 2003/0218222).

Regarding claims 4 and 5, Kawasaki et al. disclose a semiconductor device (Fig. 1) comprising an active layer (5) (line 3 of [0037]), to which elements are added (lines 3-4 of [0038]), and which is made of a semiconductor containing ZnO or $Mg_xZn_{1-x}O$ (lines 1-3 of [0038]), and a blocking member (4a, 4b, 6, 7 and 9) (lines 3-5 of [0037], [0039], and line 6 of [0050]) for blocking the active layer (5) from an atmosphere such that the atmosphere substantially does not influence a region, in which a movable charge moves, of the active layer (5). Kawasaki et al. further disclose that the active layer (5) made of a semiconductor containing ZnO is formed in an oxygen atmosphere ([0064]).

Kawasaki et al. differ from the claimed invention by not showing that nitrogen and hydrogen are added to the active layer, which is made of a semiconductor containing polycrystalline ZnO or $Mg_xZn_{1-x}O$, amorphous ZnO or $Mg_xZn_{1-x}O$, or either mixture of the polycrystalline ZnO and the amorphous ZnO or mixture of the polycrystalline $Mg_xZn_{1-x}O$ and the amorphous $Mg_xZn_{1-x}O$, wherein the active layer includes the nitrogen and hydrogen as intentionally added dopants having concentrations so that a threshold voltage of a gate voltage of the semiconductor device, when a voltage between a drain and a source region is fixed at 10V, is controlled to be substantially in a range between 0V and 3V (claim 4), wherein the active layer is formed under an atmosphere containing (i) one or more of nitrogen monoxide and nitrogen dioxide, and (ii) hydrogen peroxide (claim 5).

Goodman discloses a semiconductor device (Fig. 1) comprising an active layer (16) made of polycrystalline or amorphous ZnO (col. 2, lines 7-9).

Since both Kawasaki et al. and Goodman teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the active layer disclosed by Kawasaki et al. may comprise polycrystalline or amorphous ZnO, because a polycrystalline or amorphous semiconductor material is commonly used in manufacturing a thin film transistor to reduce processing steps, to reduce cost or to achieve a desired semiconductor device characteristics.

Further regarding claims 4 and 5, Kawasaki et al. in view of Goodman differ from the claimed invention by not showing that nitrogen and hydrogen are added to the active layer, wherein the active layer includes the nitrogen and hydrogen as intentionally

added dopants having concentrations so that a threshold voltage of a gate voltage of the semiconductor device, when a voltage between a drain and a source region is fixed at 10V, is controlled to be substantially in a range between 0V and 3V (claim 4), wherein the active layer is formed under an atmosphere containing (i) one or more of nitrogen monoxide and nitrogen dioxide, and (ii) hydrogen peroxide (claim 5).

Yan et al. disclose that high quality p-type ZnO films can be achieved using either NO or NO_2 gas as a dopant (lines 1-2 of [0036]).

Since both Kawasaki et al. and Yan et al. teach a ZnO semiconductor film, it would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the active layer disclosed by Kawasaki et al. in view of Goodman with the dopants disclosed by Yan et al., because a high quality ZnO active layer can be formed by using either NO or NO_2 gas as a dopant, and therefore nitrogen would be intentionally added to the active layer.

Further regarding claims 4 and 5, Kawasaki et al. in view of Goodman and further in view of Yan et al. differ from the claimed invention by not showing that hydrogen is added to the active layer, wherein the active layer includes the hydrogen as intentionally added dopants, the nitrogen and hydrogen having concentrations so that a threshold voltage of a gate voltage of the semiconductor device, when a voltage between a drain and a source region is fixed at 10V, is controlled to be substantially in a range between 0V and 3V (claim 4), wherein the active layer is formed under an atmosphere containing (ii) hydrogen peroxide (claim 5).

Vijayakumar et al. disclose a method for manufacturing a ZnO thin film (Title), wherein oxygen and hydrogen peroxide can be used as suitable oxidants (col. 2, lines 38-39).

Since both Kawasaki et al. and Vijayakumar et al. teach a ZnO thin film, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the ZnO active layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. may be formed under an atmosphere containing hydrogen peroxide, because oxygen and hydrogen peroxide can be used interchangeably in forming a ZnO thin film to improve characteristics of the ZnO thin film. In this case, hydrogen would be an intentionally added dopant.

Further regarding claim 4, Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. differ from the claimed invention by not showing that the active layer includes the nitrogen and hydrogen having concentrations so that a threshold voltage of a gate voltage of the semiconductor device, when a voltage between a drain and a source region is fixed at 10V, is controlled to be substantially in a range between 0V and 3V.

Wager et al. disclose a semiconductor device (Fig. 1) comprising an active layer (5) made of ZnO (line 4 of [0059]) comprising nitrogen (lines 17-23 of [0038]), wherein a threshold voltage of a gate voltage of the semiconductor device, when a voltage between a drain and a source region is fixed at about 5 to about 40V, is controlled to be in a range between about 1 V and about 20 V (lines 1-7 of [0049]).

Since both Kawasaki et al. and Wager et al. teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the nitrogen and hydrogen may have concentrations so that a threshold voltage of a gate voltage of the semiconductor device may be within the claimed range, because a threshold voltage of a field effect transistor is an important device parameter that should be optimized not to apply a high bias voltage to the field effect transistor, which would increase power consumption, and a threshold voltage of a field effect transistor can be optimized by controlling an impurity concentration, a channel layer thickness, a gate insulating layer thickness, *etc*. to improve performance of the field effect transistor. Further, claim 4 is *prima facie* obvious without showing that the claimed range of the threshold voltage achieves unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Regarding claims 6 and 7, Kawasaki et al. further disclose that the blocking member (4a, 4b, 6, 7 and 9) is made up of different blocking layers (4a, 4b, 6, 7 and 9) (claim 6), wherein a blocking layer (4b) is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2,

CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, or a solid solution containing at least two of them (lines 5-9 of [0041]) (claim 7).

Regarding claim 11, Kawasaki et al. further comprise a gate electrode (3) (line 4 of [0037]) for controlling move of a movable electric charge in the active layer (5), a gate insulating layer (4), which serves as a block layer, for insulating the active layer (5) from the gate electrode (3), a source electrode (6) connected to the active layer (5), and a drain electrode (7) connected to the active layer (5), wherein a blocking layer (4b) is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, or a solid solution containing at least two of them (lines 5-9 of [0041]).

Regarding claims 15-20, 27 and 28, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 15, 17, 19 and 27), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of [0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 16, 18, 20 and 28).

3. Claims 8, 12, 21, 22, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114) and further in view of Vijayakumar et al. (US 4,751,149) and still further in view of Wager et al. (US 2003/0218222), and then further in view of Ogawa (US 2002/0056838). The teachings

of Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. are discussed above.

Regarding claim 8, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 7 that a blocking layer (9) ([0050]) constituting the blocking layers (4a, 4b, 6, 7 and 9) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from (i) each of two electrodes (6 and 7) serving as blocking layers and connected to the active layer (5), and (ii) an insulating layer (4), which serves as a blocking layer and meets the active layer (5), for insulating the active layer (5) from a control electrode (3) for controlling move of a movable electric charge in the active layer (5).

Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. differ from the claimed invention by not showing that the blocking layer is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, …, or a solid solution containing at least two of them.

Ogawa discloses a semiconductor device (Fig. 9) comprising a blocking layer (13) (line 2 of [0181]) for a ZnO semiconductor layer (23) (lines 5-6 of [0177]), wherein the blocking layer (13) can be made of silicon nitride or silicon oxide (lines 8-11 of [0077]), which can be SiO_2.

Since both Kawasaki et al. and Ogawa teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of

Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. with the SiO_2 blocking layer disclosed by Ogawa, because SiO_2 is commonly used as an alternative to silicon nitride in manufacturing a semiconductor device to achieve a desired passivation characteristic.

Regarding claim 12, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 11 that a blocking layer (9) ([0050]) constituting the blocking layers (4a, 4b, 6, 7 and 9) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from the source electrode (6), the drain electrode (7), and the gate insulating layer (4), each of which serves as a blocking layer.

Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. differ from the claimed invention by not showing that the blocking layer is made of SiO_2, Al_2O_3, MgO, Ta_2O_5, TiO_2, ZrO_2, CeO_2, K_2O, Li_2O, Na_2O, Rb_2O, In_2O_3, La_2O_3, Sc_2O_3, Y_2O_3, …, or a solid solution containing at least two of them.

Ogawa discloses a semiconductor device (Fig. 9) comprising a blocking layer (13) (line 2 of [0181]) for a ZnO semiconductor layer (23) (lines 5-6 of [0177]), wherein the blocking layer (13) can be made of silicon nitride or silicon oxide (lines 8-11 of [0077]), which can be SiO_2.

Since both Kawasaki et al. and Ogawa teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of

Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. with the SiO_2 blocking layer disclosed by Ogawa, because SiO_2 is commonly used as an alternative to silicon nitride in manufacturing a semiconductor device to achieve a desired passivation characteristic.

Regarding claims 21, 22, 29 and 30, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 21 and 29), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of [0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 22 and 30).

4. Claims 9, 10, 13, 14, 23-26 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. (US 2003/0047785) in view of Goodman (US 4,204,217) and further in view of Yan et al. (US 2004/0061114) and further in view of Vijayakumar et al. (US 4,751,149) and still further in view of Wager et al. (US 2003/0218222), and then further in view of Kaneko et al. (US 5,166,816). The teachings of Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. are discussed above.

Regarding claims 9 and 10, Kawasaki et al. further disclose for the semiconductor device as set forth in claim 6 that a blocking layer (9) ([0050]) is made of silicon nitride, and the blocking layer (9) is so provided as to meet the active layer (5) separately from (i) each of two electrodes (6 and 7) serving as blocking layers and

connected to the active layer (5), and (ii) an insulating layer (4), which serves as a blocking layer and meets the active layer (5), for insulating the active layer (5) from a control electrode (3) for controlling move of a movable electric charge in the active layer (5).

Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. differ from the claimed invention by not showing that the blocking layer is made of resin.

Kaneko et al. disclose a semiconductor device (Fig. 6), wherein a blocking layer (61) is made of resin (col. 4, line 57), and the blocking layer (61) is so provided as to meet the active layer (54) (col. 4, lines 21-22) separately from each of two electrodes (56 and 57) (col. 4, lines 15-16) serving as blocking layers and connected to the active layer (54), and an insulating layer (53) (col. 4, line 21), which serves as a blocking layer and meets the active layer (54), for insulating the active layer (54) from a control electrode (52) (col. 4, lines 20-21) for controlling move of a movable electric charge in the active layer (54).

Since both Kawasaki et al. and Kaneko et al. teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. with the polyimide resin disclosed by Kaneko et al., because a polyimide resin is a well-known material for forming an interlayer insulating film in manufacturing a thin film transistor to achieve a desired passivation characteristic.

Regarding claims 13 and 14, Kawasaki et al. further comprise for the semiconductor device as set forth in claim 6 a gate electrode (3) (line 4 of [0037]) for controlling move of a movable electric charge in the active layer (5), a gate insulating layer (4), which serves as a block layer, for insulating the active layer (5) from the gate electrode (3), a source electrode (6) connected to the active layer (5), a drain electrode (7) connected to the active layer (5), wherein a blocking layer (9) is made of silicon nitride ([0050]), and the blocking layer (9) is so provided as to meet the active layer (5) separately from the source electrode (6), the drain electrode (7), and the gate insulating layer (4), each of which serves as a blocking layer.

Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. differ from the claimed invention by not showing that the blocking layer is made of a resin.

Kaneko et al. disclose a semiconductor device (Fig. 6) comprising a gate electrode (52) (col. 4, lines 20-21) for controlling move of a movable electric charge in the active layer (54) (col. 4, lines 21-22), a gate insulating layer (53) (col. 4, line 21), which serves as a block layer, for insulating the active layer (54) from the gate electrode (52), a source electrode (57) (col. 4, lines 15-16) connected to the active layer (54), a drain electrode (56) (col. 4, line 16) connected to the active layer (54), wherein a blocking layer (61) is made of a resin (col. 4, line 57), and the blocking layer (61) is so provided as to meet the active layer (54) separately from the source electrode (57), the drain electrode (56), and the gate insulating layer (53), each of which serves as a blocking layer.

Since both Kawasaki et al. and Kaneko et al. teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the silicon nitride blocking layer disclosed by Kawasaki et al. in view of Goodman and further in view of Yan et al. and further in view of Vijayakumar et al. and still further in view of Wager et al. with the polyimide resin disclosed by Kaneko et al., because a polyimide resin is a well-known material for forming an interlayer insulating film in manufacturing a thin film transistor to achieve a desired passivation characteristic.

Regarding claims 23-26 and 31-34, Kawasaki et al. disclose an electronic device (Figs. 8 and 9) comprising, as a switching element (T in Fig. 9), a thin film transistor (Fig. 1) ([0093] and lines 1-3 of [0096]) (claims 23, 25, 31 and 33), wherein the switching element (T) is connected to a picture element electrode (8 in Fig. 1) (line 8 of [0037]) such that an image signal is written in or read out from the picture element electrode (8) (claims 24, 26, 32 and 34).

Response to Arguments

5. Applicants' arguments filed November 11, 2010 have been fully considered but they are not persuasive.

Applicants argue that “even though Vijayakumar teaches doping using hydrogen peroxide, nowhere in Vijayakumar is there a teaching that the value of the threshold voltage is being controlled by the hydrogen dopants”. (1) This argument is not convincing, because Applicants are attacking an individual reference of Vijayakumar et al., while the prior art rejections are based on a combination of Kawasaki et al.,

Goodman, Yan et al., Vijayakumar et al. and Wager et al. In response to Applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). (2) As the Examiner stated in Non Final Office Action mailed August 17, 2010, "a threshold voltage of a field effect transistor can be optimized by controlling an impurity concentration, a channel layer thickness, a gate insulating layer thickness, *etc*.", and also it is well-known to one of ordinary skill in the art to control a threshold voltage of a field effect transistor to control a power consumption. (3) Applicants do not specifically claim a correlation between concentrations of intentionally added dopants and a threshold voltage. Further, Applicants do not claim any specific device parameters such as dimensions of the field effect transistor and ranges of the concentrations of the intentionally added dopants. (4) Also, Applicants attempt to incorporate claim limitations from the specification, which is improper as stipulated in MPEP 2111.01. (5) Further, Applicants *only* claim a semiconductor device or a method for manufacturing a semiconductor device, not a mental process of intention to incorporate intentionally added dopants to control a threshold voltage, which is not one of four categories of subject matter that are eligible for patent protection.

Applicants argue that "in other words, Wager does not teach that the doping concentration of nitrogen is chosen to control the threshold voltage, but rather he teaches that it is used to enhance the resistivity of the ZnO layer". (1) This argument is

not convincing, because Applicants suggest that there should be a specific and exact teaching in the prior art of correlation between concentrations of intentionally added dopants and a threshold voltage even when the threshold voltage depends on a lot of other device parameters. (2) Also, this argument appears to suggest that concentrations of intentionally added dopants are the *only* parameters that would determine the recited threshold voltage, while Applicants do not specifically claim ranges of the concentrations of the intentionally added dopants. Rather, as the Examiner stated in Non Final Office Action mailed August 17, 2010, there are other device parameters such as a channel layer thickness and a gate insulating layer thickness that would change a threshold voltage. (3) Wager et al. disclose a threshold voltage within the claimed range. (4) Further, Applicants cannot claim an intention to achieve a desired threshold voltage *only* by controlling the concentrations of intentionally added dopants without claiming other critical and essential parameters in the practice of the invention such as a channel layer thickness and a gate insulating layer thickness, *etc*.

Applicants argue that "as the Examiner admitted, there are other factors that can be used to control the threshold voltage, so that it is not obvious to use the doping of nitrogen to control the threshold voltage", and that "the threshold voltage range disclosed in Wager may result from any other factor, not from the concentration of nitrogen, let alone the concentration of hydrogen". (1) The Examiner notes that Applicants acknowledged that Wager et al. disclose a threshold voltage within the claimed range. (2) As stated above, Applicants argue that Applicants' claims are

directed to intention to control a threshold voltage of a field effect transistor by *only* the concentrations of intentionally added dopants, which is not a patentable subject matter. Applicants' arguments above are basically that a semiconductor device should be manufactured with the same intention as Applicants' of controlling the concentrations of intentionally added dopants to control a threshold voltage to meet the claim limitations of claim 4. However, Applicants omitted essential and critical device parameters in the practice of the invention such as dimensions of the field effect transistor and a material of the gate insulating layer in claim 4 that would determine the concentrations of intentionally added dopants to achieve the recited threshold voltage. (3) Also, Applicants do not specifically claim that *only* the concentrations of intentionally added dopants are controlled to achieve the recited threshold voltage. (4) Controlling a threshold voltage of a field effect transistor is well-known to one of ordinary skill in the art as Applicants acknowledged in arguments above.

Applicants argue that "in addition, Applicant respectfully submits that the range for the threshold voltage of the gate voltage cited in claim 4 achieves unexpected results relative to prior art ranges, thus the cited prior art's teachings would not have made it obvious to intentionally add nitrogen and hydrogen dopants having concentrations so that a threshold voltage of a gate voltage of the semiconductor device is controlled to be substantially in a range between 0V and 3V, as alleged by the Examiner, see p. 6 of the Office Action". (1) This argument is not convincing, because Applicants do not provide any evidence of unexpected results relative to prior art ranges. (2) Also, this argument is not in agreement with Applicants' previous arguments

where Applicants acknowledged that Wager et al. disclose a threshold voltage within the claimed range. (3) Further, see responses above regarding claiming an intention to control a threshold voltage.

Applicants argue that "Wager discloses properties of a TFT shown in Fig. 1, which has no protective layer". This argument is again based on attacking an individual reference of Wager et al. See responses above regarding attacking individual references.

Applicants argue that "in the invention of claim 4, nitrogen and hydrogen are so doped that the number of the free electrons as carriers is reduced", and that "this makes it possible to obtain a threshold voltage of the TFT in a practical range of 0V to 3V, which is away from the expected range of large negative values (around -30V)". These arguments are not convincing, especially because Wager et al. disclose a threshold voltage within the claimed range. It appears that Applicants' arguments may be true for certain device parameters such as dimensions of the field effect transistor or concentrations of intentionally added dopants, but may not be applied to in general with Wager et al. providing a counterexample. Therefore, it appears that other device parameters critical and essential in the practice of the invention may not have been claimed in claim 4, which would not be enabling.

The Examiner suggests Applicants to claim specific parameters such as ranges of the concentrations of intentionally added dopants and dimensions of the semiconductor device, or a specific device structure such as a bilayer structure of layer

4 in Fig. 2 of current Application, because a threshold voltage depends on various device parameters.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
December 18, 2010
/KENNETH A PARKER/
Supervisory Patent Examiner, Art Unit 2815